

SONY COMPUTER ENTERTAINMENT ANNOUNCES WORLD'S FASTEST 128 Bit CPU "EMOTION ENGINE™" FOR THE NEXT GENERATION PLAYSTATION®

TOKYO, March 2, 1999 - Sony Computer Entertainment Inc. is pleased to announce the co-development with Toshiba Corp. of the 128 bit CPU ("EE", or "Emotion Engine™") for use in the next generation of PlayStation®. In order to process massive multi-media information at the fastest possible speeds, data bus, cache memory as well as all registers are 128 bits; this is integrated on a single chip LSI together with the state of the art 0.18 micron process technology. The development of a full 128-bit CPU is the first of its kind in the world.

Not only will this new CPU have application for games, but it will be the core media processor for future digital entertainment applications, and has a vastly superior floating point calculation capability compared to the latest personal computers. The new CPU incorporates two 64-bit integer units (IU) with a 128-bit SIMD multi-media command unit, two independent floating point vector calculation units (VU0, VU1), an MPEG 2 decoder circuit (Image Processing Unit/IPU) and high performance DMA controllers onto one silicon chip. The massive combined performance of this CPU permits complicated physical calculation, NURBS curved surface generation and 3D geometric transformations, which are difficult to perform in real time with PC CPUs, to be performed at high speeds.

In addition, by processing the data at 128-bits on one chip, it is possible to process and transfer massive volumes of multi-media data. CPUs on conventional PCs have a basic data structure of 64 bits, with only 32 bits on recent game consoles. The main memory supporting the high speed CPU uses the Direct Rambus® DRAM in two channels to achieve a 3.2GB/second bus bandwidth. This equates to four times the performance of the latest PCs that are built on the PC-100 architecture.

By incorporating the MPEG 2 decoder circuitry on one chip, it is now possible to simultaneously process high-resolution 3D graphics data at the same time as high quality DVD images. The combination of the two allows the introduction of a new approach to digital entertainment and real-time graphics and audio processing.

With a floating point calculation performance of 6.2GFLOPS/second, the overall calculation performance of this new CPU matches that of a super computer. When this is applied to the processing of geometric and perspective transformations normally used in the calculation of 3D computer graphics (3DCG), the peak calculation performance reaches 66 million polygons per second. This performance is comparable with that of high-end graphics workstations (GWS) used in motion picture production.

Rambus is a registered trademark of Rambus Inc.

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For further information, please contact your local PR Manager.

Sony Computer Entertainment Europe is responsible for the distribution and software development for the PlayStation®, the world's number one selling (CD-based) video game system and has offices around Europe, the Middle East, Australia and New Zealand promoting the PlayStation® and its software in more than 65 territories.

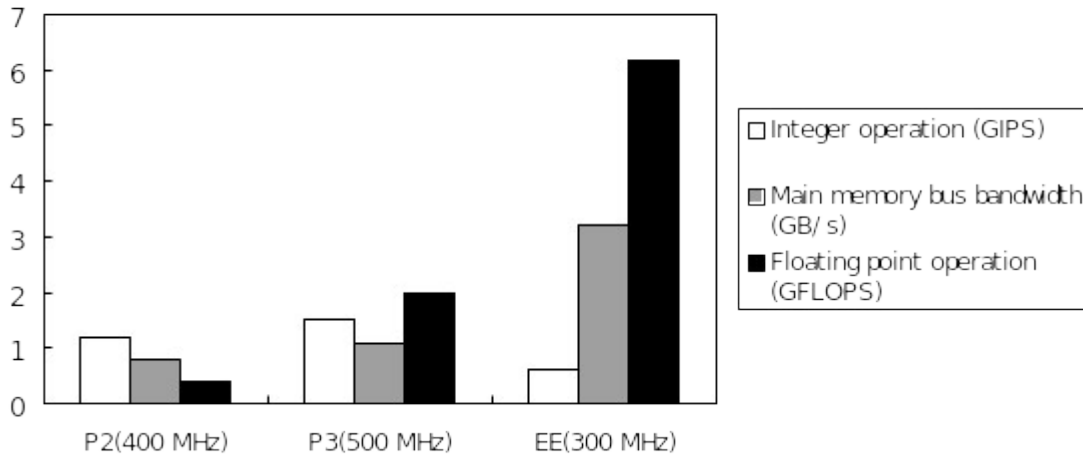
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Emotion Engine Features and General Specifications

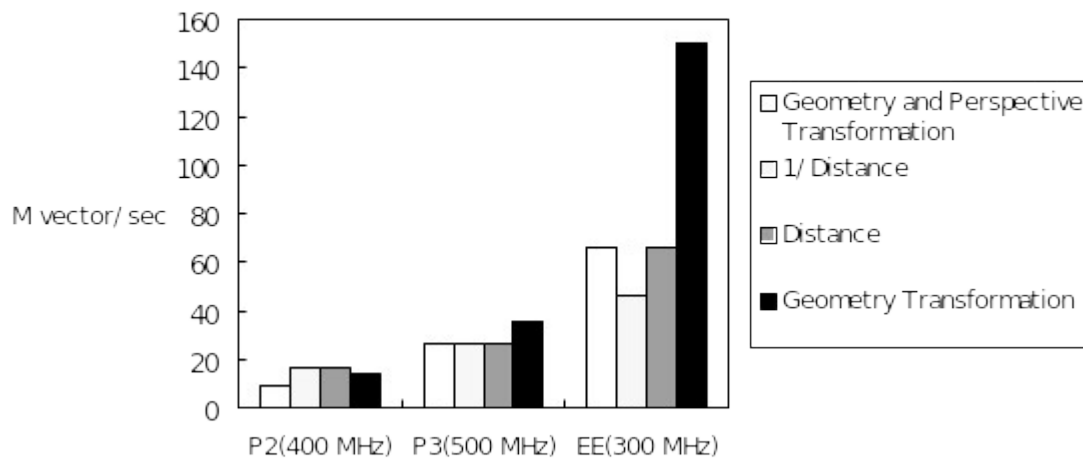
CPU core	128 bit RISC (MIPS IV-subset)
Clock Frequency	300MHz
Integer Unit	64bit (2-way Superscalar)
Multimedia extended instructions	107 instructions at 128 bit width
Integer General Purpose Register	32 at 128 bit width
TLB	48 double entries
Instruction Cache	16KB (2-way)
Data Cache	8KB (2-way)
Scratch Pad RAM	16KB (Dual port)
Main Memory	32MB (Direct RDRAM 2ch@800MHz)
Memory bandwidth	3.2GB/sec
DMA	10 channels
Co-processor1	FPU (FMAC x 1, FDIV x 1)
Co-processor2	VU0 (FMAC x 4, FDIV x 1) Micro Memory (I:4KB D:4KB)
Vector Processing Unit	VU1 (FMAC x 5, FDIV x 2) Micro Memory (I:16KB D:16KB)
Floating Point Performance	6.2GFLOPS
Geometry	
+ Perspective Transformation	66Million Polygons/sec
+ Lighting	38Million Polygons/sec
+ Fog	36Million Polygons/sec
Curved Surface Generation (Bezier)	16Million Polygons/sec
Image Processing Unit	MPEG2 Macroblock Layer Decoder
Image Processing Performance	150Million Pixels/sec
Gate width	0.18 micron
VDD Voltage	1.8 V
Power Consumption	15 Watts
Metal Layers	4
Total Transistors	10.5 Million
Die Size	240 mm ²
Package	540pin PBGA

<Reference Data>

Peak Performance



Floating point vector performance *



*) 4 dimensional calculation to single precision floating point.
 EE performance based on measured data. For P2 and P3, theoretical maximum values based on manufacturer's figures and other published data.